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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,930	01/29/2004	Shigetaka Kasuga	60188-761	1865

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EXAMINER	
CUTLER, ALBERT H	

ART UNIT	PAPER NUMBER
2622	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/765,930	KASUGA, SHIGETAKA	
	Examiner	Art Unit	
	Albert H. Cutler	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 7-9* is/are rejected.

7)☒ Claim(s) *2-6 and 10-15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is responsive to application 10/765,930 filed on January 29, 2004. Claims 1-15 are pending in the application and have been examined by the examiner.

Information Disclosure Statement

2. The Information Disclosure Statements (IDS) mailed on January 29, 2004 and October 4, 2006 were received and have been considered by the examiner.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Gowda et al.(U.S. Patent 6,115,066).

Consider claim 1, Gowda et al. teach:

A solid state imaging device(figures 3 and 4) using N-type MOS transistors alone as transistors included therein(Column 5, lines 12-13, figure 4), comprising:

a pixel unit(image sensor, 20, figure 3) composed of a plurality of pixels(30) arranged in a two-dimensional matrix(see figure 3), each of said pixels(30) including a photoelectric converting element(26, figure 4) for generating charge in response to light(26 is a photodiode, column 4, lines 23-25.) and an amplifying element(23, figure 4) for outputting, as an analog signal, a voltage signal corresponding to said charge generated by said photoelectric converting element(FET 23 provides a signal directly related to(i.e. an amplified signal) the charge on the photodiode, column 6, lines 19-22.);

a selection signal line(15, figure 3) provided correspondingly to each pixel row(see figure 3) of said pixel unit(20);

a comparison/storage unit(40 and 42, figure 3) provided correspondingly to each pixel column(see figure 3) of said pixel unit(20) for converting, into a digital signal, said analog signal output from said amplifying element(23) included in each pixel(30) belonging to a pixel row selected in said pixel unit(30, see figure 3) and for storing said digital signal(Each pixel row contains an ADC(40) for converting the analog signal into a digital signal, column 6, lines 22-26. This digital signal is then stored in a register(42), column 6, lines 24-26.);

a scanner(44, figure 3) for selecting and reading said digital signal stored in said comparison/storage unit in time series(column 6, line 28 through column 7, line 20); and

an amplifier(44, figure 3) for amplifying said read digital signal and outputting said amplified digital signal to the outside(The "logic block"(44) acts as a differential amplifier

by subtracting the reset signals from the data output from the comparison/storage unit, column 3, line 64 through column 4, line 1. Data is output from logic block(44) to image storage and processing electronics(i.e. the outside), column 7, lines 17-21.).

6. Claims 7, 8, and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim et al.(U.S. Patent 6,423,957).

Consider claim 7, Kim et al. teach:

A solid state imaging device(figure 4), comprising:

a pixel unit("pixel array", 20) formed on a semiconductor substrate and outputting, as an analog signal, a voltage signal corresponding to light(Column 2, lines 52-57); and

an AD converter(30, figure 4) formed on said semiconductor substrate(The device is a CMOS device, column 2, lines 49-51.) and converting said analog signal output from said pixel unit into a digital signal(column 2, lines 55-57), wherein transistors included in said pixel unit and said AD converter are all N-type MOS transistors(The AD converter(30) comprises a comparator(32), a double buffer(40), and a ramp voltage generator(31), figure 4. The AD converter(30) of figure 4 contains the same parts as the AD converter(30) of figure 1. These parts are detailed in figure 2, where a pixel(200) from the pixel unit is shown, and the comparator(320) and double buffer(400) of the AD converter(30) are also shown. All of these devices clearly contain NMOS transistors alone, see figure 2.), and

said AD converter(30) includes a booster circuit(See figure 2. The double buffer(400) is part of the AD converter(30), and is externally connected to a booster circuit in the form of a transistor connected to "PRECHARGE" and a power supply.).

Consider claim 8, and as applied to claim 7 above, Kim et al. further teach:

said booster circuit includes a transistor whose source or drain is connected to power potential(see figure 2, claim 7 rationale), and a voltage not less than said power potential is applied to a gate of said transistor(The booster circuit is used to pre-charge the bit line using the potential of the power supply.).

Consider claim 9, and as applied to claim 7 above, Kim et al. further teach:

said AD converter(30) includes, in addition to said booster circuit, any or all of a comparator(32, figure 4), a memory(40, figure 4), a pulse generator(31, figure 4) and a counter generator("Count Signal", figure 4).

Allowable Subject Matter

7. Claims 2-6, and 10-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter:

Consider claim 2, the closet prior art, Gowda et al. (US 6,115,066) teaches a comparison/storage unit(see claim 1 rationale). However, Gowda et al. do not teach or fairly suggest that the comparison circuit is comprised of three inverter circuits including three N-type MOS transistors alone or serially connected, or that the resistance of various transistors is increased or decreased to increase the rise speed or fall speed of the inverters.

Consider claim 10, the closest prior art, Kim et al.(6,423,957) teaches of a comparator(32, figure 4, 320, figure 2), and of a booster circuit(see claim 7 rationale). However, Kim et al. do not teach of fairly suggest that the comparator has an inverter circuit containing a booster circuit.

Consider claim 11, the closest prior art, Kim et al.(6,423,957) teaches of a comparator(32, figure 4, 320, figure 2), and of a booster circuit(see claim 7 rationale). However, Kim et al. do not teach of fairly suggest that the comparator has an inverter circuit containing a booster circuit, or that the inverter circuit has a second transistor formed above a well region independent of other well regions.

Consider claim 12, the closest prior art, Kim et al.(6,423,957) teaches of a memory(40, 400) and a booster circuit(see claim 7 rationale). Kim et al. further teach that said memory(400) includes a plurality of switches(M5-M8, figure 2). However, Kim et al. do not teach of fairly suggest that said memory includes a capacitor or an output amplifier connected to a booster circuit.

Consider claim 14, the closest prior art, Kim et al.(6,423,957) teaches of a scanner("Column Select Signal", figure 2), a pulse generator(31, figure 4), and a

booster circuit(see claim 7 rationale). However, Kim et al. do not teach of fairly suggest that the pulse generator includes a plurality of inverter circuits serially connected to one another, or that the inverter circuit disposed at the ultimate stage includes a booster circuit.

Consider claim 15, the closest prior art, Kim et al.(6,423,957) teaches of a counter generator("COUNT SIGNAL", figure 4), a pulse generator(31 figure 4), and a booster circuit(see claim 7 rationale). However, Kim et al. do not teach of fairly suggest that the said counter generator includes a plurality of inverter circuits each having a booster circuit.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kwon et al.(U.S. Patent 6,633,335) detail the same circuit configurations as Kim et al. Oh(U.S. Patent 5,636,169) teach of a precharge voltage generator containing multiple inverter circuits(see figure 2). Hanzawa et al.(U.S. Patent Application Publication 2003/0123313) teach of using NMOS transistors in a precharge voltage circuit, and driving said circuit using the voltage of the power supply(paragraph 0081).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert H. Cutler whose telephone number is (571)-270-1460. The examiner can normally be reached on Mon-Fri (7:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ngoc-Yen Vu can be reached on (571)-272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AC

NGOC-YEN VU
SUPERVISORY PATENT EXAMINER